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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/688,073 | 10/17/2003 | Yoshihiro Okada | 81784.0287 | 8162 |

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HOGAN & HARTSON L.L.P.
1999 AVENUE OF THE STARS
SUITE 1400
LOS ANGELES, CA 90067

| EXAMINER | |
|---|---|
| YEUNG LOPEZ, FEIFEI | |
| ART UNIT | PAPER NUMBER |
| 2826 | |
| MAIL DATE | DELIVERY MODE |
| 09/15/2008 | PAPER |

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/688,073 | OKADA ET AL. | |
| | Examiner | Art Unit | |
| | FEI FEI YEUNG LOPEZ | 2826 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *7/23/08*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-6* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## DETAILED ACTION

### *Continued Examination Under 37 CFR 1.114*

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 7/23/2008 has been entered.

### *Claim Objections*

2. Claims 5-6 are objected to because of the following informalities:

3. Regarding claim 5, "the semiconductor region of reverse conductive type" lacks antecedent basis.

4. Regarding claim 6, the limitation “the third reverse conductive semiconductor region” lacks antecedent basis.

5. Appropriate correction is required.

### *Claim Rejections - 35 USC § 102*

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 1-2, 4, and 6 are rejected under 35 U.S.C. 102(b) as being anticipated by Wada (US Patent 5,220,185).

8. Regarding claim 1, Wada teaches a solid image capturing element, comprising: a plurality of vertical shift registers (layers 54 in fig. 5) arranged to each correspond to a column of a plurality of light receiving pixels (layer 51) in a matrix arrangement, a horizontal shift register (layer 55) provided on an output side of the plurality of vertical shift registers, and an output section (layer 56) provided on an output side of the horizontal shift register, wherein a semiconductor region of one conductive type (p type layer above layer 11 in fig. 1) is formed closer to a surface (the bottom surface of layer 11) of a semiconductor substrate of one conductive type, while a semiconductor region of reverse conductive type (n layer directly above the p layer) is formed in a deeper portion (deeper into the substrate from the bottom surface of the substrate) than the semiconductor region of one conductive type, and a first semiconductor region (layer 22) and a second semiconductor region of the opposite conductive type (layer 20) and having a higher dopant concentration (n+ has higher concentration than n) than that of the first semiconductor region are formed in the semiconductor region of reverse conductive type, the horizontal shift register (areas in layer 13 and to the right of layer 13 in fig. 1) is formed in the first semiconductor region; and the output section (output amplifier or charge detecting section 21 and 56 in figs. 1 and 5, respectively) is formed in the second semiconductor region.

FIG. 5

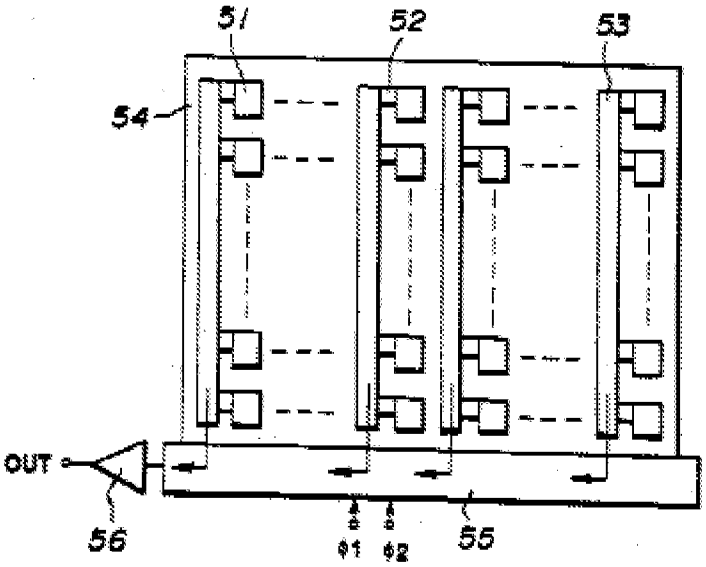
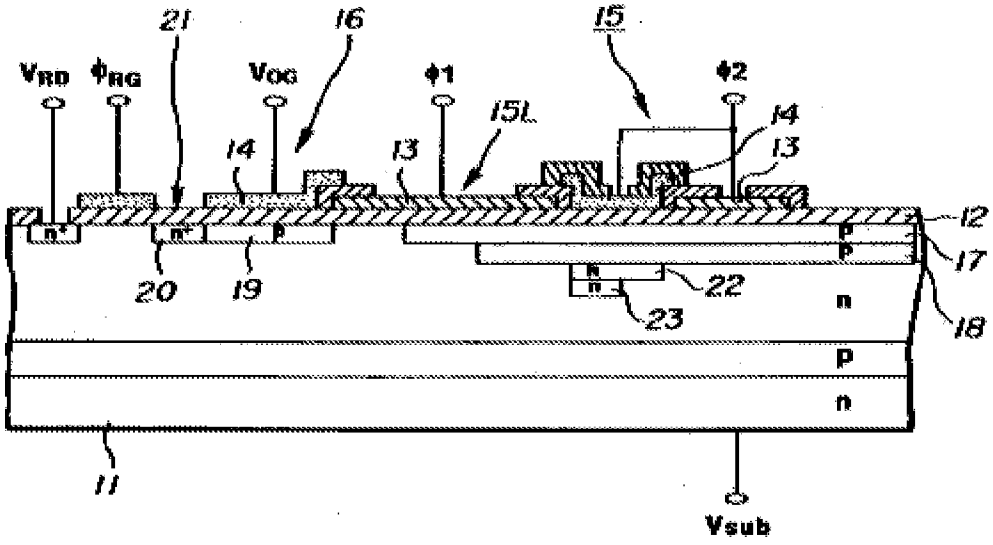


FIG.1




9. Regarding claim 2, Wada teaches the solid image capturing element according to claim 1, further comprising: an output gate (VOG in fig. 1) formed on the semiconductor substrate at a boundary between the horizontal shift register and the output section.

10. Regarding claim 4, Wada teaches a method for manufacturing a solid image capturing element having a plurality of vertical shift registers arranged to each correspond to a column of a plurality of light receiving pixels in a matrix arrangement, a horizontal shift register provided on an output side of the plurality of vertical shift registers, and an output section provided on an output side of the horizontal shift register (see rejection in claim 1), comprising: a first step of forming closer to a surface (the bottom surface of layer 11 in fig. 1) of a conductive semiconductor substrate, a first

reverse conductive semiconductor region (n type layer 23 in fig. 1, which has reverse conductive type than the p type layer above the n type bottom layer) having a first dopant concentration; a second step of forming in a deeper portion (further away from the bottom surface of the substrate) in the conductive semiconductor substrate than the conductive semiconductor region, a second reverse conductive semiconductor region (n+ layer 20) having a second dopant concentration which is higher than the first dopant concentration (n+ has higher concentration than n); and a third step of forming the horizontal shift register (areas in layer 13 and to the right of layer 13, see fig. 1) on the first reverse conductive semiconductor region and the output section (layer 21) on the second reverse conductive semiconductor region.

11. Regarding claim 6, Wada teaches the method for manufacturing a solid image capturing element according to claim 4, wherein a dopant is doped in a stepwise manner (steps formed by two rectangular patches of doped regions—regions 20 and 23, see fig. 1) to the first reverse conductive semiconductor region and the second reverse conductive semiconductor region, and doping of the dopant is performed commonly (when the n layer above the p type well, which is above layer 11, is made) at least once to the first reverse conductive semiconductor region, the second reverse conductive semiconductor region.

12. Claims 1, 3-4 are rejected under 35 U.S.C. 102(b) as being anticipated by Morimoto (US Patent 6,426,238 B1).

13. Regarding claim 1, Morimoto teaches a solid image capturing element, comprising: a plurality of vertical shift registers (layer 102 in fig. 6) arranged to each

correspond to a column of a plurality of light receiving pixels (layer 106) in a matrix arrangement, a horizontal shift register (layer 103) provided on an output side of the plurality of vertical shift registers, and an output section (fig. 3G) provided on an output side of the horizontal shift register, wherein a semiconductor region (upper surface region of p substrate layer 120 in fig. 3G) of one conductive type is formed closer to a surface of a semiconductor substrate of one conductive type, while a semiconductor region of reverse conductive type (n- layer 121) is formed in a deeper portion (away from bottom surface of substrate 120) than the semiconductor region of one conductive type, and a first semiconductor region (n layer 12) and a second semiconductor region (n+ layer 127) having a higher dopant concentration than that of the first semiconductor region are formed in the semiconductor region of reverse conductive type (n- layer 121), the horizontal shift register is formed in the first semiconductor region; and the output section is formed in the second semiconductor region.

FIG. 6

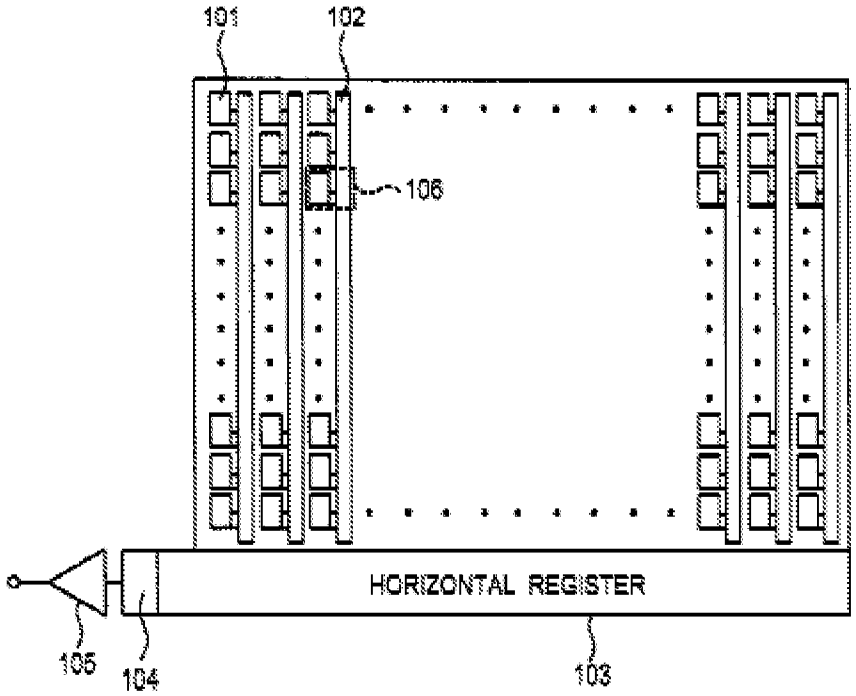
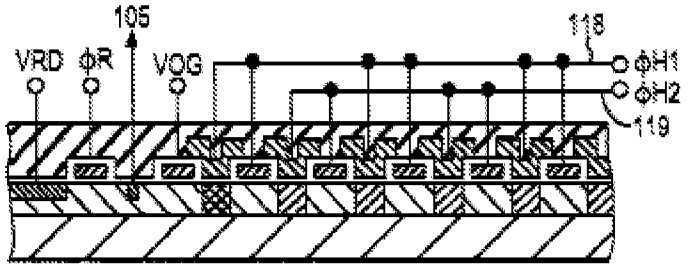


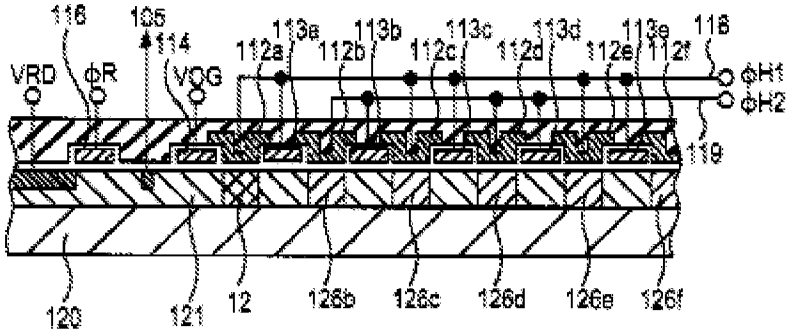

FIG. 3G




14. Regarding claim 3, Morimoto teaches the solid image capturing element according to claim 1, wherein in the semiconductor region of reverse conductive type (n-layer 121), a third semiconductor region (n- layer 126b) having a lower dopant

concentration than that of the first semiconductor region (n layer 12) is formed, and plurality of vertical shift registers are formed in the third semiconductor region.

FIG. 2




15. Regarding claim 4, Morimoto teaches a method for manufacturing a solid image capturing element having a plurality of vertical shift registers arranged to each correspond to a column of a plurality of light receiving pixels in a matrix arrangement, a horizontal shift register provided on an output side of the plurality of vertical shift registers, and an output section provided on an output side of the horizontal shift register (see rejection in claim 1), comprising: a first step of forming closer to a surface of a conductive semiconductor substrate, a first reverse conductive semiconductor region (layer 121 in fig. 3G) having a first dopant concentration; a second step of forming in a deeper portion (away from p substrate 120) in the conductive semiconductor substrate than the first reverse conductive semiconductor region, a second reverse conductive semiconductor region (n+ layer 127) having a second dopant concentration which is higher than the first dopant concentration; and a third

step of forming the horizontal shift register (e.g. layer 126a) on the first reverse conductive semiconductor region and the output section (output amplifier 105) on the second reverse conductive semiconductor region.

***Claim Rejections - 35 USC § 103***

16. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

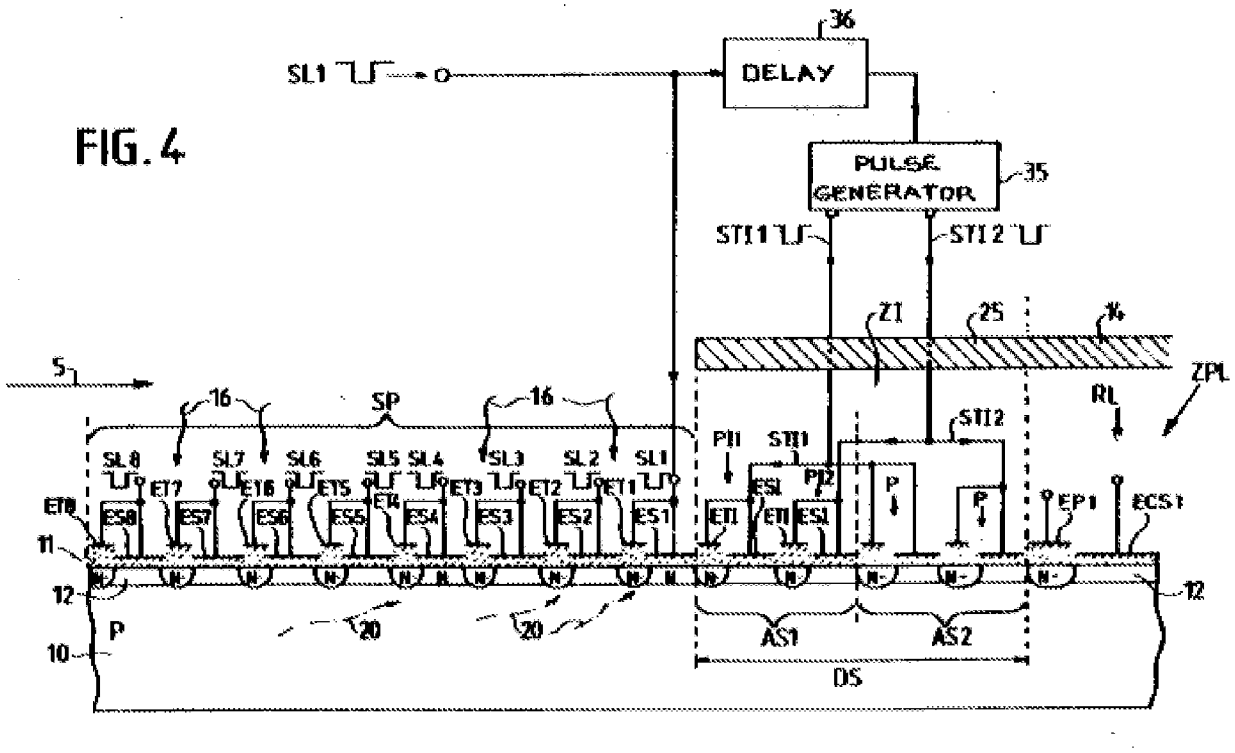
17. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

18. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Morimoto (US Patent 6,426,238 B1) as applied to claim 4 above, and further in view of Cazaux (US Patent 5,283,451).

19. Regarding claim 5, Morimoto remains as applied in claim 4. However, Morimoto does not teach the method for manufacturing a solid image capturing element according to claim 4, further comprising: a fourth step of forming in the first semiconductor region of reverse conductive type, a third reverse, conductive semiconductor region having a third dopant concentration which is lower than the first dopant concentration, wherein at

the fourth step, the plurality of light receiving pixels and the plurality of vertical shift registers are formed in the third semiconductor region. In the same field of endeavor, Cazaux teaches forming in a first semiconductor region of reverse conductive type (layer 12 in fig. 4, which is analogous to layer 121 in fig. 3G of Morimoto), a third reverse, conductive semiconductor region (n- layer 20 in fig. 4) having a third dopant concentration which is lower than the first dopant concentration, wherein at the fourth step, a plurality of light receiving pixels and a plurality of vertical shift registers are formed in the third semiconductor region (see fig. 4) for the benefit of eliminating smearing (column 6). Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to include in the first semiconductor region of reverse conductive type, a third reverse, conductive semiconductor region having a third dopant concentration which is lower than the first dopant concentration, wherein at the fourth step, the plurality of light receiving pixels and the plurality of vertical shift registers are formed in the third semiconductor region for the benefit of eliminating smearing.




### *Response to Arguments*

20. Applicant's arguments with respect to claims 1-6 have been considered but are moot in view of the new ground(s) of rejection.

### *Conclusion*

Any inquiry concerning this communication or earlier communications from the examiner should be directed to FEI FEI YEUNG LOPEZ whose telephone number is (571)270-1882. The examiner can normally be reached on 7:30am-5:00pm Monday to Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sue Purvis can be reached on 571-272-1236. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Leonardo Andújar/
Primary Examiner, Art Unit 2826

FYL
/Feifei Yeung-Lopez/
Examiner, Art Unit 2826